ARTICLE

Metal Contact Engineering and Registration-Free Fabrication of Complementary Metal-Oxide Semiconductor Integrated Circuits Using Aligned Carbon Nanotubes

Chuan Wang, Koungmin Ryu, Alexander Badmaev, Jialu Zhang, and Chongwu Zhou*

Department of Electrical Engineering, University of Southern California, Los Angeles, California 90089, United States

ABSTRACT Complementary metal-oxide semiconductor (CMOS) operation is very desirable for logic circuit applications as it offers rail-to-rail swing, larger noise margin, and small static power consumption. However, it remains to be a challenging task for nanotube-based devices. Here in this paper, we report our progress on metal contact engineering for n-type nanotube transistors and CMOS integrated circuits using aligned carbon nanotubes. By using Pd as source/drain contacts for p-type transistors, small work function metal Gd as source/drain contacts for n-type transistors, and evaporated SiO_2 as a passivation layer, we have achieved n-type transistor, PN diode, and integrated CMOS inverter with an air-stable operation. Compared with other nanotube n-doping techniques, such as potassium doping, PEI doping, hydrazine doping, *etc.*, using low work function metal contacts for n-type nanotube devices is not only air stable but also integrated circuit fabrication compatible. Moreover, our aligned nanotube platform for CMOS integrated circuits shows significant advantage over the previously reported individual nanotube platforms with respect to scalability and reproducibility and suggests a practical and realistic approach for nanotube-based CMOS integrated circuit applications.

KEYWORDS: aligned carbon nanotubes · field-effect transistors · low work function metal contact · n-type transistors · CMOS integrated circuits

Single-walled carbon nanotubes offer extraordinary electrical properties,[1−5] such as high intrinsic carrier mobility and current-carrying capacity and are envisioned as a potential candidate for the next generation beyond silicon transistor and integrated circuit applications. They have been used extensively to demonstrate ballistic and high-mobility transistors[6−8] and various integrated logic circuits and ring oscillators.[9−13] For logic circuit applications, it is of course desirable to have complementary metal-oxide semiconductor (CMOS) operation since it gives rail-to-rail swing, larger noise margin, and, most importantly, small static power consumption. However, the CMOS operation gives rise to difficulties when using nanotube-based devices since nanotubes typically exhibit p-type behavior in ambient environments. In order to convert the nanotube devices into n-type, many approaches have been reported in the literature, such as vacuum annealing, potassium doping, chemical doping, and electrostatic gating.[10,14−16] However, all of the works mentioned above have their own drawbacks. For example, the vacuum annealing and potassium doping techniques are not air stable, while chemical doping, even though can be air stable and sounds appealing, is not yet compatible with the state-of-the-art integrated circuit fabrication process.

Alternatively, n-type transistors can also be achieved by metal contact engineering. It is well-known that Palladium (Pd), with a large work function, will align with the valence band of the carbon nanotubes and form ohmic contacts for holes. Consequently, the devices with Pd conacts will exhibit p-type behavior. Thus it is natural to hypothesize that by using metals with small work function as the electrodes, it should be possible to obtain n-type conduction from the nanotubes as well. Recently, significant advance has been made on the above-mentioned topic by using small work function metals, such as scandium (Sc) and Yttrium (Y), to demonstrate CMOS inverters and diodes on individual carbon nanotube.[17−19] This technique nevertheless has some drawbacks. For example, in order to use individual nanotube for transistors, it is inevitably necessary to identify the semiconducting nanotubes beforehand, and the ensuing device fabrication process will also require locating of one specific nanotube and e-beam writing, which make the process not scalable. Moreover, individual nanotube devices are typically more vulnerable and can give large device-to-device variation.

*Address correspondence to chongwuz@usc.edu.

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Using parallel aligned carbon nanotubes can be one straightforward solution to the above-mentioned problems faced by individual nanotube devices. Recently, several groups including our own have reported the growth of massively aligned nanotubes on sapphire or quartz substrates.[20−24] Based on the aligned nanotubes, we have proposed a nanotube-on-insulator platform and demonstrated high-performance submicrometer transistors and CMOS integrated circuits, such as inverter, NAND, and NOR using both chemical and potassium doping.[25−27] The advantages of aligned nanotubes include registration-free fabrication, high device yield, and small device-to-device variation, which are exactly the shortcomings of the individual nanotube devices. Of course, the aligned nanotube platform also faces difficulty, which is the removal of metallic nanotubes. However, this is easily solved by using our automated electrical breakdown process, as described in our previous publications.[27]

In this paper, we apply metal contact engineering to our existing aligned nanotube platform. Combining small work function metal Gadolinium (Gd) for n-type contact[28] and large work function metal Pd for p-type contact, we have demonstrated registration-free fabrication of air-stable n-type aligned nanotube transistors, PN-junctions, and CMOS integrated inverters. Our aligned nanotube approach for CMOS integrated circuits shows significant advantage over individual nanotube platforms with respect to scalability and reproducibility and suggests a practical and realistic approach for nanotube-based CMOS integrated circuit applications.

RESULTS AND DISCUSSION

Figure 1a illustrates the fabrication process of the back-gated n-type nanotube transistors, which begins with aligned nanotube synthesis on quartz substrates using chemical vapor deposition (CVD) (see Methods Section). The scanning electron microscopy (SEM) image of the aligned nanotubes on quartz substrate is shown in the inset of Figure 1a. After synthesis, the nanotubes are then transferred to Si/SiO_2 substrates using a facile gold film and thermal releasing tape method, as reported in our previous publications.[26,27] Following the nanotube transfer is the device fabrication process. SiO_2 with a thickness of 500 nm is used to act as the back-gate dielectric, and the source and drain electrodes are patterned by photolithography. In order to achieve nanotube transistors with n-type behavior in air, metals with small work function need to be used, which will allow the Fermi level of the electrodes to align with the conduction band of the carbon nanotubes and thus gives ohmic contact for electrons and a large schottky barrier for holes. In this paper, Gd with a work function of ∼3.1 eV[28] is used as the metal contact, and 70 nm Gd is deposited by thermal evaporation followed by the lift-off process to form the source and drain metal contacts. Figure 1a shows optical microscope images of the back-gated n-type aligned nanotube transistors after the fabrication. The schematic diagram and SEM image of the devices are shown in Figure 1b and c, respectively.

The electrical properties of the devices are characterized, and all the measurements are carried out in air. For the aligned nanotube devices, due to the presence of both metallic and semiconducting nanotubes, metallic nanotube removal technique, such as electrical breakdown, is necessary. More information about the electrical breakdown process can be found in the literature[29] and our previous publications.[26,27] Figure 1d shows the transfer ($I_D - V_G$) characteristics for a typical n-type nanotube transistor ($L = 4\ \mu$m, $W = 8\ \mu$m) measured at $V_D = 1$ V before and after electrical breakdown. Before breakdown, the device exhibits on/off ratio of around 2. After electrical breakdown, the on/off ratio is improved to around 1000 with a trade-off with the on current. Figure 1e shows the transfer characteristics of the device after electrical breakdown measured under different drain voltages, and Figure 1f shows output characteristics ($I_D - V_D$) of the device measured under different gate voltages. From the transfer characteristic, one can find that the transistor exhibits clear n-type behavior. For the output characteristics, it appears to be very linear for V_D smaller than 1 V (S1, Supporting Information), indicating that ohmic contacts are formed between the Gd electrodes and the nanotubes. Under higher V_D, the device exhibits saturation behavior which indicates nice field-effect operation.

Even though the above-mentioned back-gated transistor with Gd contacts only approach is straightforward and simple, there are some shortcomings. First, due to the adsorption of oxygen on nanotubes, the nanotubes are always heavily p-doped, so the devices sometimes exhibit ambipolar behavior instead of predominant n-type behavior as shown in the Supporting Information (S2). Second, Gd (and other small work function metals) is susceptible to air and moisture, will be oxidized relatively easily in air, and the resistivity will increase greatly in a few days after device fabrication. Finally, since the transferred aligned nanotubes cover the entire substrate, oxygen plasma is necessary to remove the unwanted nanotubes outside the device channel region to achieve accurate channel length and width and to remove the possible leakage in the devices. However, Gd can be attacked by O_2 plasma, so the unwanted nanotube etching has to be done prior to the electrode patterning, which adds one more step of alignment mark patterning to the fabrication process.

Because of the three reasons mentioned above, it is crucial to develop a passivation technique for Gd contacts, and we propose to use the e-beam evaporated SiO_2 for this purpose. The schematic diagram of the passivated n-type device fabrication process is

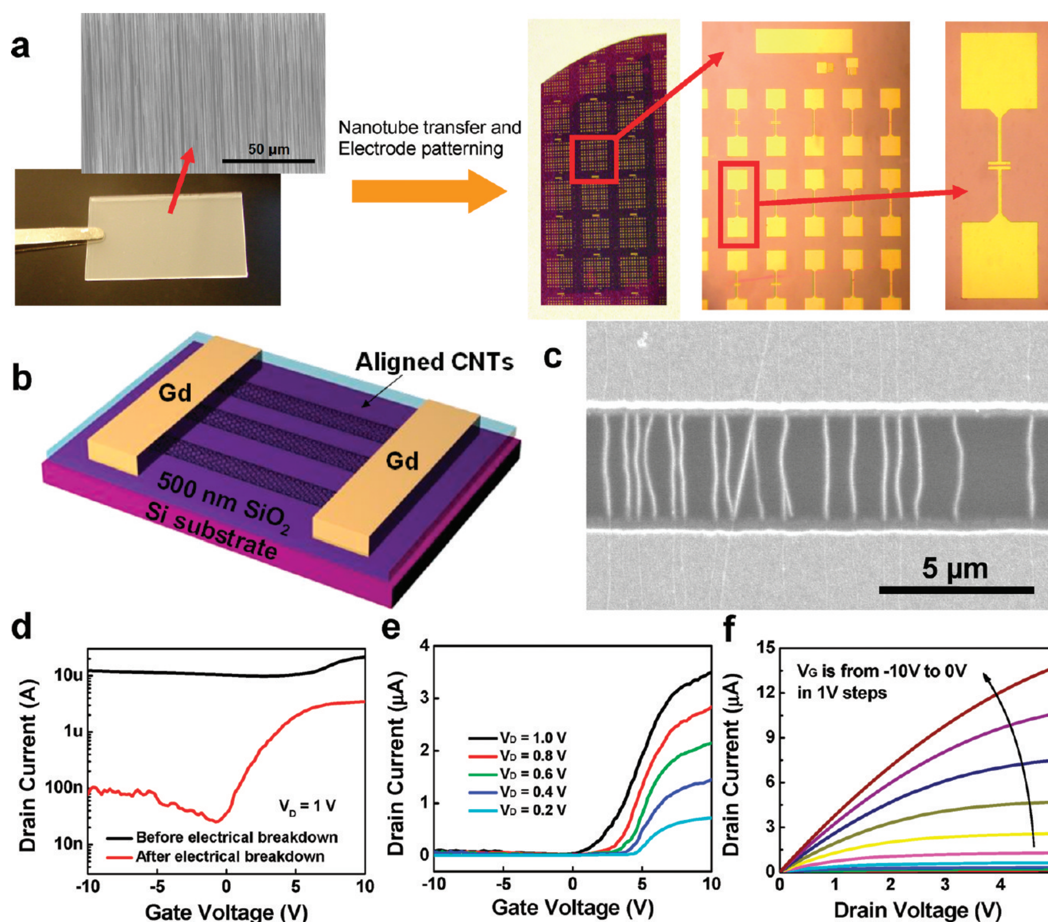

Figure 1. Fabrication of the back-gated n-type nanotube transistors and their electrical properties. (a) Simplified process flow of the n-type nanotube transistor fabrication including aligned nanotube synthesis on quartz substrate (left) (inset: SEM image of the aligned nanotubes), transfer to Si/SiO_2 substrate, and Gd metal electrode patterning by photolithography and lift-off process. The optical photographs of the completed chip and a typical device are shown in the right. (b) Schematic diagram and (c) SEM image of the n-type aligned nanotube transistor with Gd metal contacts. (d) Transfer ($I_D - V_G$) characteristics of a typical n-type nanotube transistor (L = 4 μm, W = 8 μm) measured at V_D = 1 V before and after electrical breakdown. (e) Transfer characteristics of the same device measured under different drain voltages after electrical breakdown. (f) Output ($I_D - V_D$) characteristics of the same device measured under different gate voltages.

shown in Figure 2a. In brief, the device fabrication begins with the individual back-gated aligned nanotube transistors with Ti/Pd contacts. The benefit of using individual back-gated structures is the individual control of each transistor in a nanotube circuit, and the fabrication process of the individual back-gated Ti/Pd-contacted device is discussed in the Methods Section. The transfer characteristics of the pristine device (L = 2 μm, W = 5 μm) after electrical breakdown are shown in Figure 2b, which shows p-type behavior as expected since Pd is known to form ohmic contacts for holes due to its large work function. E-beam lithography is used to pattern source/drain extensions with 500 nm extension into the channel and with width equal to the transistor channel width. Gd contacts are then deposited by thermal evaporation and lift-off process. In this Ti/Pd contact pads plus Gd source/drain extension configuration, the effect from the Gd extensions should be more dominant since the Gd extensions are closer to the nanotube channel than the Ti/Pd contact pads.

Figure 2c shows the transfer characteristics of the same devices shown in Figure 2b after the Gd contacts deposition. Comparing Figure 2c with b, one can find the transition from p-type behavior to ambipolar behavior. It is likely that the nanotubes are heavily p-doped in air due to the adsorption of oxygen on the nanotubes, so the devices exhibit ambipolar behavior instead of predominant n-type behavior. SiO_2 passivation is demonstrated to be effective for suppressing the p-type conduction of the ambipolar devices, as discussed below, and the SiO_2 capping layer is deposited by e-beam evaporation. The transfer characteristics of the device with Gd source/drain extensions before and after passivation are shown in Figure 2d. The figure indicates that after passivation the p-type conduction is suppressed, and the n-type conduction becomes predominant. The suppression of p-type conduction is likely due to the desorption of adsorbed oxygen in the high-vacuum chamber and to the ensuing SiO_2 passivation, which makes the nanotubes more intrinsic. We have also tested poly(methyl

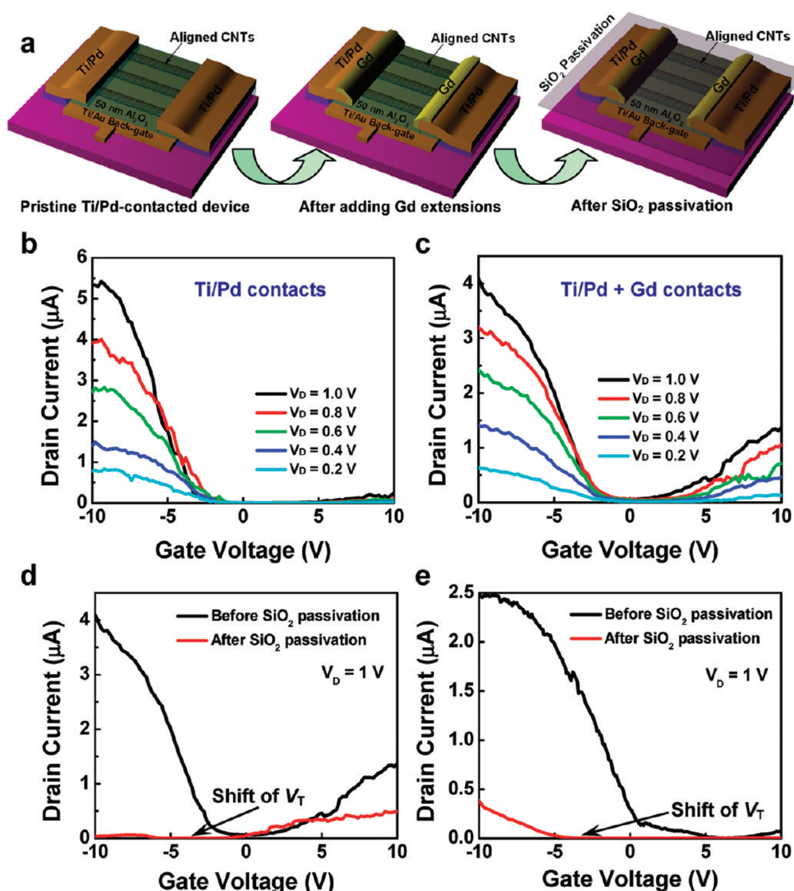

Figure 2. Electrical properties of the passivated transistor with Gd source/drain extensions. (a) Schematic diagram showing the fabrication process of the passivated individual-gated n-type transistor. Starting from the individual back-gated transistor with Ti/Pd metal contacts, Gd source and drain extensions are patterned by e-beam lithography, followed by SiO_2 passivation deposited by e-beam evaporation. (b) Transfer characteristics of an individual back-gated transistor ($L = 2\ \mu m$, $W = 5\ \mu m$) with Ti/Pd metal contacts. (c) Transfer characteristics of the same device after adding Gd source/drain extensions by e-beam lithography. (d) Transfer characteristics of the same device with Ti/Pd plus Gd source/drain extensions before and after SiO_2 passivation measured at $V_D = 1$ V. (e) Transfer characteristics of a typical device with only Ti/Pd metal contacts before and after SiO_2 passivation measured at $V_D = 1$ V.

methacrylate) (PMMA) passivation for the Gd-contacted devices and have found that it is ineffective for suppressing the p-type conduction of the pristine ambipolar devices as opposed to the effective SiO_2 passivation. More information can be found in the Supporting Information (S3), and a similar observation is also reported in the literature.[10] Moreover, we have also observed that the n-type on-current degraded after the SiO_2 passivation, and this is observed from most devices tested. The degradation of the n-type on-current might be related to either the oxidation of Gd in air during the device fabrication process, before the SiO_2 passivation layer is deposited, or the SiO_2 passivation, which leads to increased carrier scattering at the oxide/nanotube interface.

SiO_2 passivation is also performed to Pd-contacted transistors and the results are shown in Figure 2e. Suppression of p-type conduction is also observed from these devices. However, the device remains to be p-type after passivation. This is because Pd aligns with the valence band of carbon nanotubes, so the schottky barrier for electrons is still significant even though the nanotubes themselves become more intrinsic, and thus the electron conduction is still much weaker compared with hole conduction. Moreover, from both Gd- and Pd-contacted transistors shown in Figure 2d and e, one can observe the shift of threshold voltage, which indicates the shift of Fermi level of carbon nanotubes after passivation. Before passivation, the adsorption of oxygen in air leads to the charge transfer to the nanotubes, resulting in p-doping and shifting the Fermi level of the nanotubes to close to the valence band.[10,30−33] After passivation, due to the desorption of oxygen, the Fermi level of the carbon nanotubes shifts from close to the valence band to approximately the middle of the bandgap. As a consequence, the threshold voltage shifts toward a more negative value for both Gd-contacted n-type and Pd-contacted p-type devices.

Using similar approach, diode devices can also be achieved. The schematic diagram and the optical microscope and SEM images (with artificial color) of

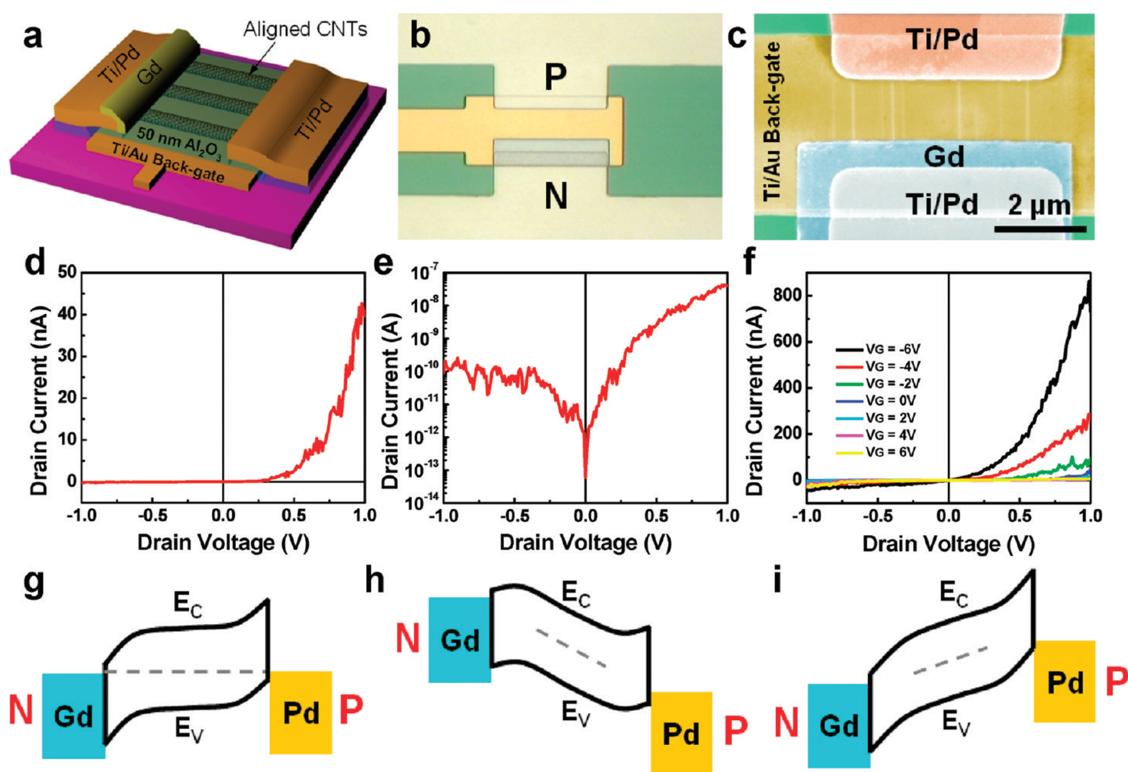

Figure 3. Aligned nanotube PN junction based on Pd and Gd metal contacts. (a) Schematic diagram of a PN junction based on Pd and Gd metal contacts. (b) Optical microscope image of a typical PN diode device. (c) SEM image (with artificial color) of a typical PN diode device. (d, e) *I* − *V* characteristics of the diode device plotted in linear (d) and logarithm (e) scale, respectively. (f) *I* − *V* characteristics measured under different gate voltages. (g) Energy band diagrams showing the equilibrium, (h) forward-bias, and (i) reverse-bias of the diode, respectively.

the diode device are shown in Figure 3a−c, respectively. The device fabrication is similar to the above-mentioned passivated individual-gated n-type transistor, except that the Gd extension is only patterned to one of the electrodes. In this case, Pd will align with the valence band and form ohmic contact for holes at one terminal, and Gd will align with the conduction band and form ohmic contact for electrons at the other terminal. This will result in the PN junction, and the corresponding energy band diagram in equilibrium, forward bias, and reverse bias are shown in Figure 3g−i, respectively. With positive voltages applied to the p-side, the device operates in the forward-bias region, and the barrier height reduces. Consequently, current flow increases exponentially with the applied positive bias voltage. In contrast, with negative voltages applied to the p-side, the device operates in the reverse-bias region, and the barrier height increases, preventing the current from flowing. The above-mentioned processes translate into the two-terminal *I* − *V* characteristic of the PN-junction shown in Figure 3d and e (linear and logarithm scale, respectively), which exhibits clear rectifying behavior. Moreover, by changing the gate voltages applied to the diode, the engery band of the nanotube in the channel can be modulated, and this results in the modulation of the current. The gate dependence of the *I-V* characteristics of the diode is plotted in Figure 3f.

Furthermore, an integrated CMOS inverter is demonstrated with different source drain metal contacts for optimum pull-up and pull-down performance. The schematic diagram and optical microscope image of the integrated CMOS inverter are shown in Figure 4a and b. This CMOS inverter features an individual Ti/Au back-gate, a Pd-contacted p-type device and a Gd-contacted n-type device. Figure 4c is the SEM image (with artificial color) showing the n-type branch of the CMOS inverter, which clearly highlights the aligned carbon nanotubes in the channel, original Ti/Pd metal contacts, Gd source/drain extensions, and Ti/Au back-gate. The transfer characteristics of the p-type pull-up branch and n-type pull-down branch of the CMOS inverter are shown in Figure 4d and e, respectively, and the corresponding energy band diagrams are shown as the insets. From their transfer characteristics, we can further derive the output resistance of the p-type and n-type transistors at different gate voltages. Based on the derived output resistances and by treating these two transistors as a voltage divider, we can obtain the simulated inverter voltage transfer characteristics (VTC), as shown in Figure 4f. To measure the VTC of the inverter, 3 V is applied as the V_{DD}, and the input voltage is swept from 0 to 5 V. The measurement results are compared with the simulation results obtained from Figure 4f, and the corresponding

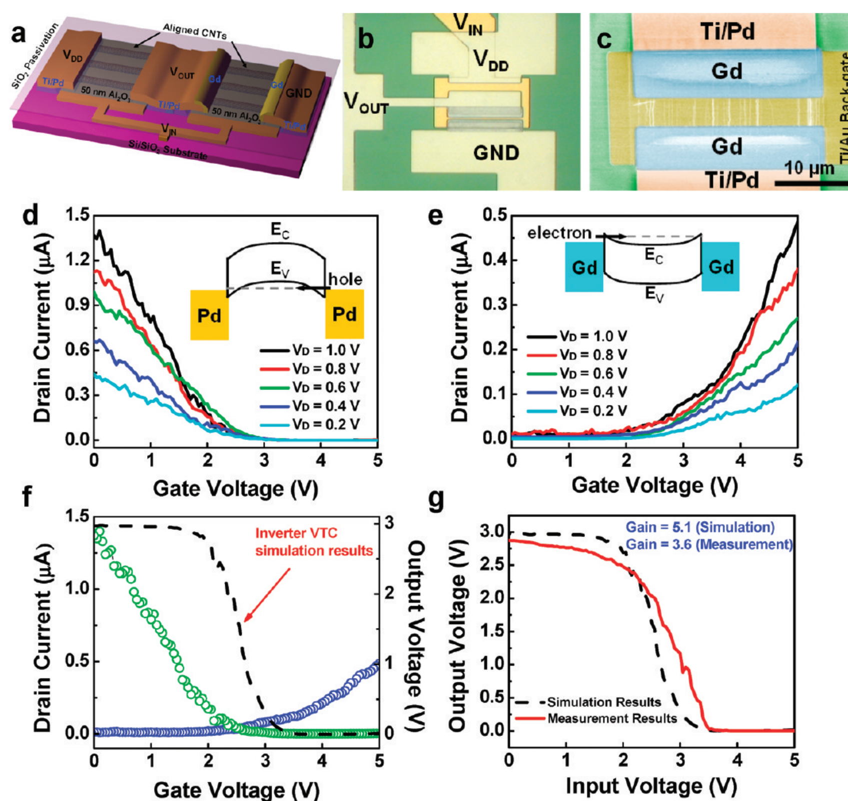

Figure 4. Integrated nanotube CMOS inverter based on Pd and Gd metal contacts. (a) Schematic diagram and (b) optical microscope image of the integrated CMOS inverter with different source drain metal contacts, Pd for p-type branch, and Gd for n-type branch. (c) SEM image (with artificial color) showing the n-type branch of the CMOS inverter with Gd source/drain extensions. (d) Transfer characteristics of the p-type pull-up branch and (e) n-type pull-down branch of the CMOS inverter, respectively. Inset: energy band diagram of the corresponding devices. (f) Transfer characteristics of the p- and n-type transistors and the simulated inverter voltage transfer characteristic. (g) Measured and simulated voltage transfer characteristics of the CMOS inverter.

inverter voltage transfer characteristics are plotted in Figure 4g. From the figure, one can find that the measurement results match the simulation results well. As input voltage increases, the output voltage switches from V_{DD} to 0, indicating nice CMOS inverter operation. The switching threshold happens at around V_{IN} = 2.65 V when both NMOS and PMOS are simultaneously on, and this results in a maximum gain of 3.6. The inverter switching threshold of 2.65 V is slightly larger than one-half of the input sweeping range (2.5 V), which is because the Pd-contacted p-type device is more conductive than the Gd-contacted n-type device, resulting in an inverter with stronger pull-up strength.

In summary, we have reported significant progress on metal contact engineering for air-stable n-type transistors, PN junctions, and CMOS integrated circuits using horizontally aligned carbon nanotubes. This scalable approach can serve as the building block for future nanotube-based CMOS integrated circuit applications.

METHODS

Aligned Carbon Nanotube Synthesis. Aligned single-walled carbon nanotubes are grown on the quartz substrates with evaporated iron catalysts defined by photolithography. The samples are annealed in air at 900 °C for 2 h, and CVD is used to grow aligned nanotubes between the catalyst islands with CH_4 (2000 sccm) and H_2 (300 sccm) as the feeding gases at 900 °C.

Nanotube Transfer. 100 nm gold film is deposited onto the quartz substrates containing nanotubes, and the thermal releasing tape (Nitto Denko) is used to peel off the gold film together with the nanotubes, which is then pressed with a polydimethylsiloxane (PDMS) stamp against the targeting substrates preheated on a hot plate at 140 °C for 10 s. After this process, the thermal tape is peeled off with the PDMS stamp. Finally, oxygen plasma is used to clean the tape residue, and gold etchant is used to remove the gold film, leaving only aligned nanotubes on the target substrate.

Individual Back-Gated Transistor Fabrication. Ti/Au back-gate is patterned by photolithography and lift-off process, and 50 nm Al_2O_3 high-κ dielectric is deposited on top of the Ti/Au back-gate by atomic layer deposition (ALD). Aligned nanotubes are then transferred to the ALD layer using the method mentioned previously. After nanotube transfer, the source/drain electrodes are patterned by photolithography, and 5 Å Ti and 70 nm Pd are deposited by e-beam evaporation followed by the lift-off process to form the source and drain metal contacts. Finally, one more step of photolithography plus O_2 plasma is used to remove the unwanted nanotubes outside the device channel region in order to achieve accurate channel length and width and to remove the possible leakage in the devices.

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Supporting Information Available: Linear region output characteristics of the Gd-contacted nanotube transistors (S1); N-type and ambipolar Gd-contacted aligned nanotube transistors in ambient environment (S2); Gd-contacted aligned nanotube transistors with PMMA passivation (S3). This material is available free of charge *via* the Internet at http://pubs.acs.org.

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